III-V nanowires for energy: low power nanoelectronics and other opportunities.

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Energy crisis in ICT

- 3% of the world’s electricity supply
- 2% of total greenhouse gas emissions

Data Center farm

- Reducing the power consumption in MOS device is the key since most of the operating power for servers and storage is consumed by microprocessors and memories.
Scaling of MOS device: power issue

- **Motivation**: pursue transistor miniaturization to the extreme scaling.
- **Enhanced electrostatic control** -> new 3D architecture.

**Proposed answer:**

- **Performance**: High mobility channel
- **Energy efficiency**: GAA (Low Ioff)
- **III-V (Reduced VDD)**

Size scaling
Realization of III/V NW arrays

Issues associated to nanoelectronic applications:

- Localization/density/diameter
- Quick integration in standard process flow, CMOS compatible
- Si platform integration (high lattice mismatched).
T-D: III-V NWs on Si

III-V layer grown on Si(100)

GaAs (200-700nm)

Si (100)

MOCVD 300mm
(CEA-LTM Grenoble
T. Baron et al.)

Patterning + RIE

GaAs

Si(100)

GaAs 400nm

500nm

A. Lecestre, N. Mallet et al.
Hetero structured III-V / Si NWs by T-D

**EBL: Resist nanodots**

**Chlorine plasma etching: GaAs nanowires**

**Fluorine plasma etching**
GaAs-Si heterostructured NWs with resist

**HF + Plasma O2**
GaAs-Si hetero structured nanowires
B-U: Positioning and Yield of NW arrays

> Direct integration of high mobility materials on silicon by surface nanostructuration

T-D: Nano-hole structuration in thermal SiO₂ layer.

B-U growth: VLS growth of GaAs NW by MBE

> High yield of NW arrays on Si

> Key parameters:
  - Hole diameter
  - In and As fluxes
  - Temperature

InAsSb
We developed a CMOS compatible process for the integration of high-mobility InAs nanowires on Silicon.

**In-situ annealing with As**

+ HF 5%
+ H₂ plasma

＞ InAs nanowires are epitaxially grown on Si(111)

＞ Strain and dislocations are locked at the InAs-Si interface
Integration issue on III-V: gate oxide and contacts

> 2 main roadblocks in III/V MOSFETs

- Low resistive S/D contacts (CMOS comp)
- Gate oxide integration (low defects)

**Low Resistive contacts on 3D NWs:**
- Ni$_2$GaAs alloy (RTA anneal)
- CMOS-compatible technology
- Contact resistivity: $2 \times 10^{-4} \ \Omega \cdot \text{cm}^2$

**High-k gate oxide:**
- Conformal Al$_2$O$_3$ layer by ALD
- Surface preparation: sulfur passivation + in-situ cleaning
- Interface defect density: $5 \times 10^{12} \ \text{cm}^{-2} \cdot \text{eV}^{-1}$
- Oxide trapped charge: $2 \times 10^{12} \ \text{cm}^{-2}$
Toward the full device demonstration

> Low power demo targeted:

- VDD ~ 0.5V
- Physical gate length < 15nm
Other Opportunities: Thermoelectrics

> What is thermoelectricity?

- A direct conversion of temperature gradients into electricity (Seebeck effect)

> Why is it interesting?

- Everywhere energy is used a part is “lost” in heat (computers, cars, industry …)

⇒ The idea is to “collect” these loses

> Nano-generators?

- Better performances than bulk (improved ZT) due to a lower thermal conductivity in NWs
- Interesting for “local” production
Other Opportunities: Thermoelectrics

> Using material engineering integrated on Si …

BiSb NWs

> … and developing new nanoscale Topological Insulators (near zero electrical resistance + high thermal resistance = high ZT) for improved thermoelectric devices
Conclusion

> III-V nanowires devices for energy:
  - low power nanoelectronics: vertical III/V nanowires FETs: from NWs patterning to integration issues.
  - Other opportunities: Thermoelectric …

People involved in this thematic at LAAS:
 Nicolas Mallet, Daya Dhungana, Aurélie Lecestre, Fuccio Cristiano, Pier Francesco Fazzini, Emmanuel Scheid, Julien Pezard, Sébastien Plissard, Guilhem Larrieu
Other Opportunities: Solar cells

Using III-V nanowires integrated on Si to build tandem solar cells

State of the art for NW solar cells

Using processes developed in LAAS for direct integration on silicon