LAAS Days
Research & Technology

III-V nanowires for energy: low power nanoelectronics and other opportunities.

Guilhem Larrieu

guilhem.larrieu@laas.fr

Energy crisis in ICT

Data Center farm

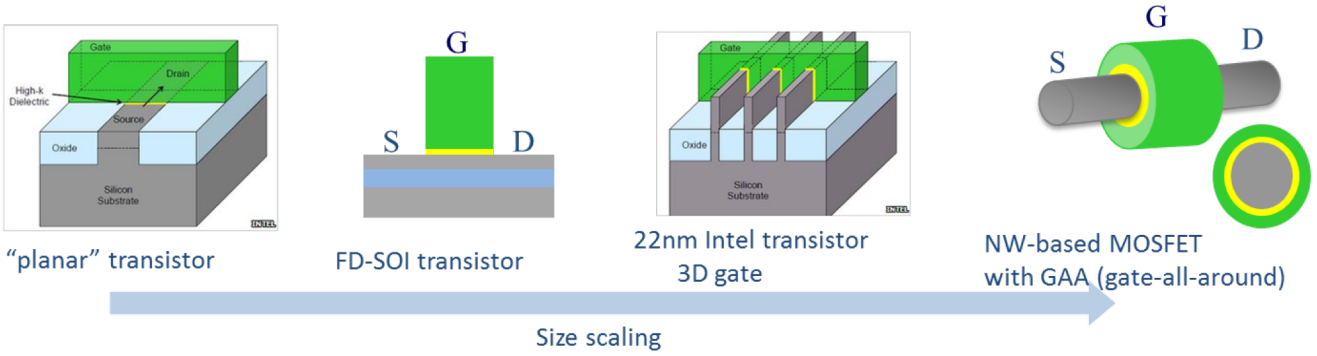
- 3% of the world's electricity supply
- 2 % of total greenhouse gas emissions

- Reducing the power consomption in MOS device is the key since most of the operating power for servers and storage is consumed by microprocessors and memories.

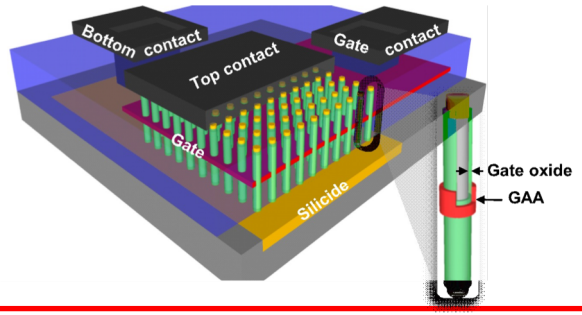
Scaling of MOS device: power issue

> Motivation: pursue transistor miniaturization to the extreme scaling.

> Enhanced electrostatic control -> new 3D architecture.



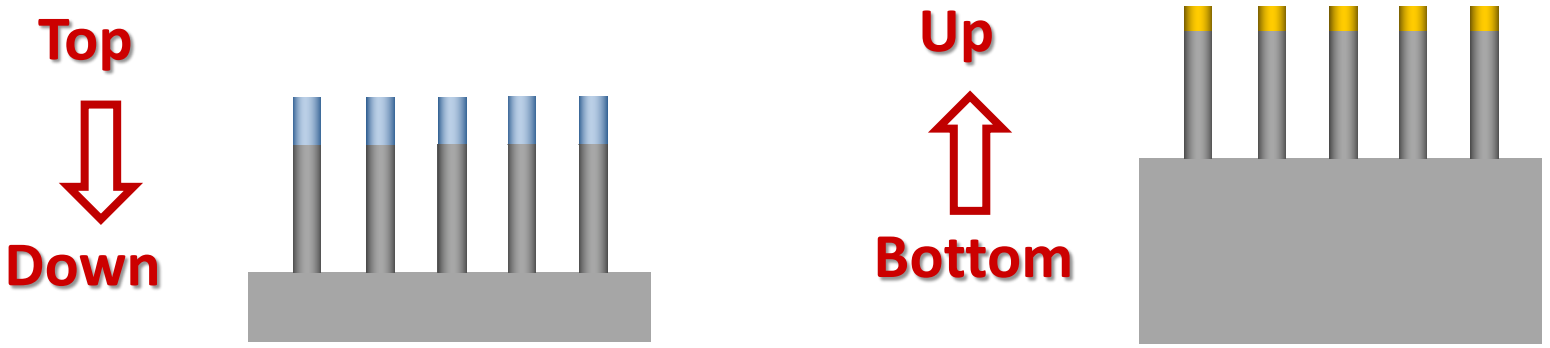
> Proposed answer:



Performance :
High mobility channel

Energy efficiency: GAA (Low Ioff) III-V (Reduced VDD)

Realization of III/V NW arrays

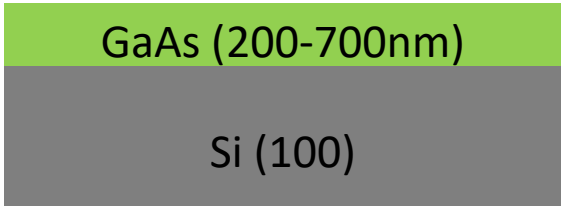


Issues associated to nanoelectronic applications:

- Localization/density/diameter
- Quick integration in standard process flow, CMOS compatible
- Si platform integration (high lattice mismatched).

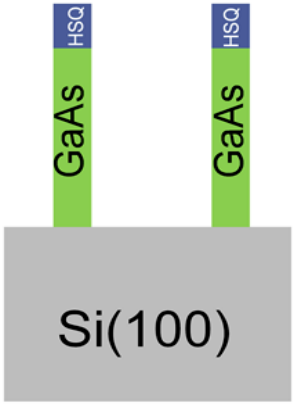
T-D: III-V NWs on Si

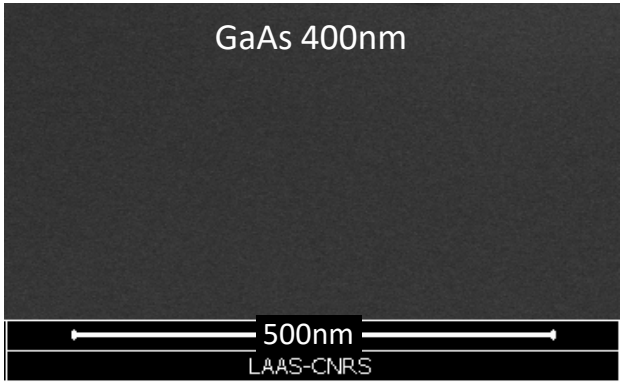
III-V layer grown on Si(100)

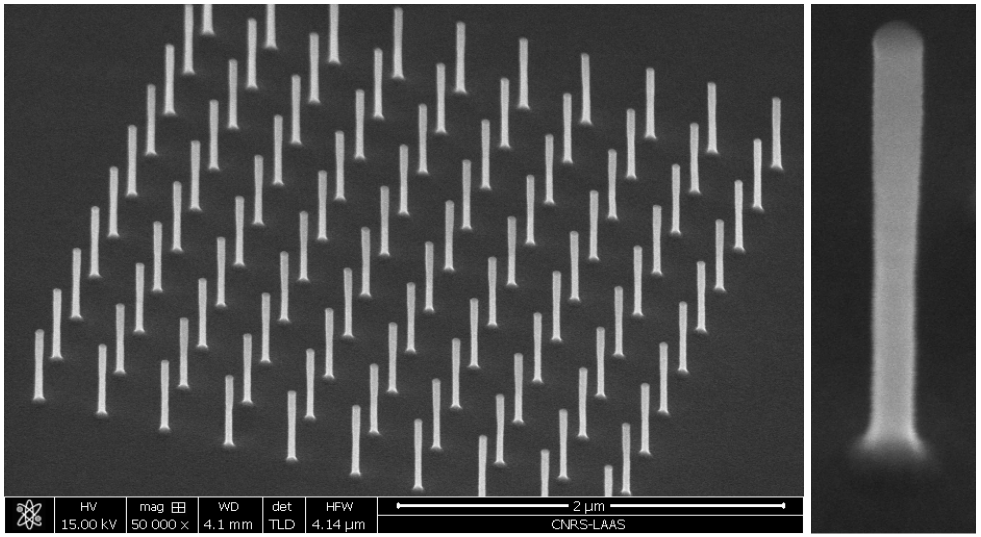


MOCVD 300mm
(CEA-LTM Grenoble
T. Baron *et al.*)

Patterning
+ RIE



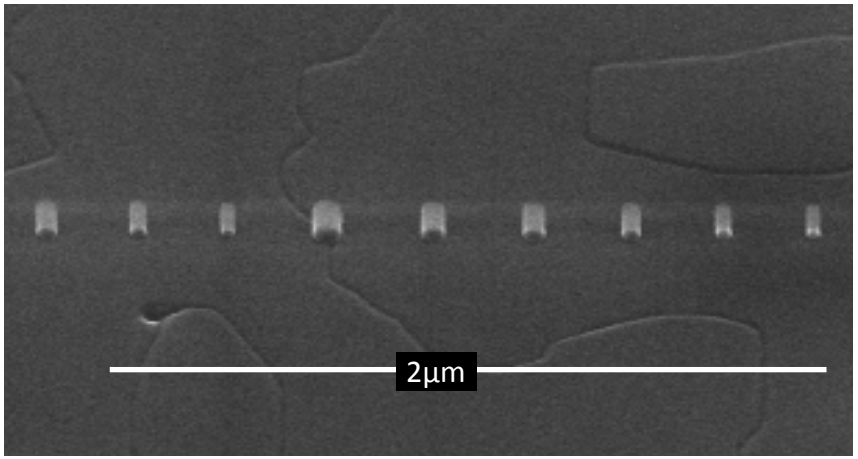




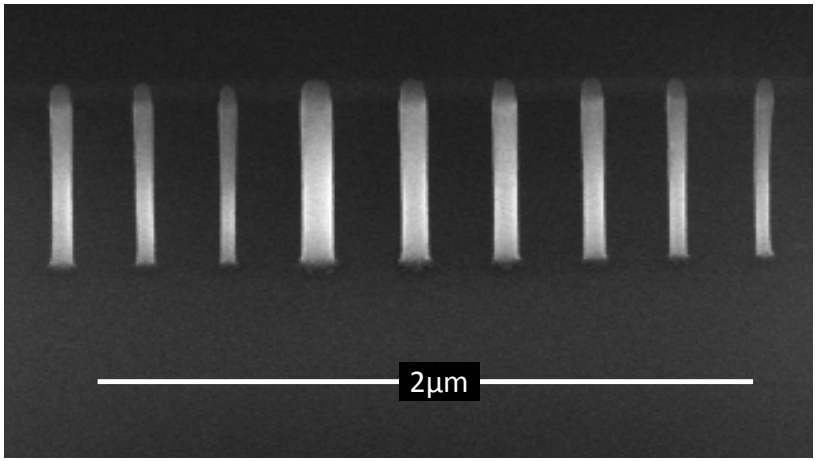
A. Lecestre, N. Mallet *et al.*

Hetero structured III-V / Si NWs by T-D

EBL: Resist nanodots

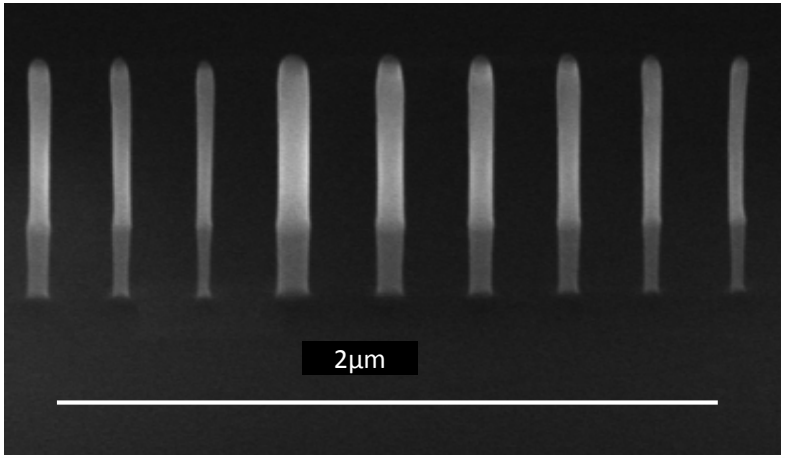


Chlorine plasma etching: GaAs nanowires



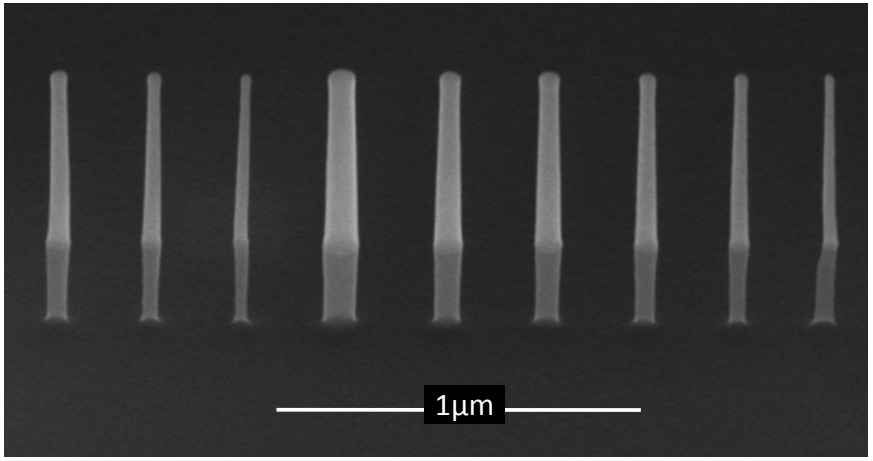
Fluorine plasma etching

GaAs-Si heterostuctured NWs with resist



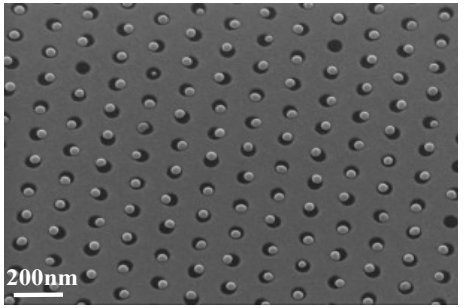
HF + Plasma O2

GaAs-Si hetero structured nanowires

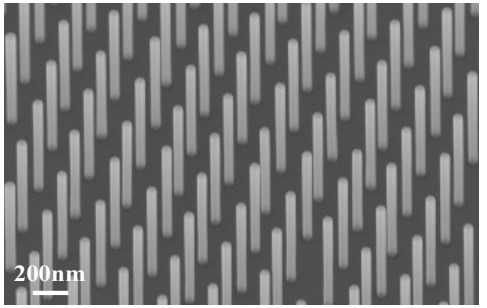


B-U: Positioning and Yield of NW arrays

- Direct integration of high mobility materials on silicon by surface nanostructuration



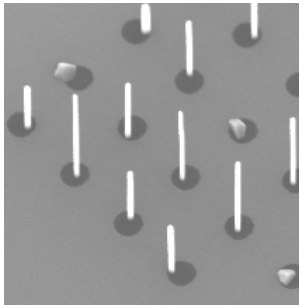
T-D: Nano-hole structuration in thermal SiO_2 layer.



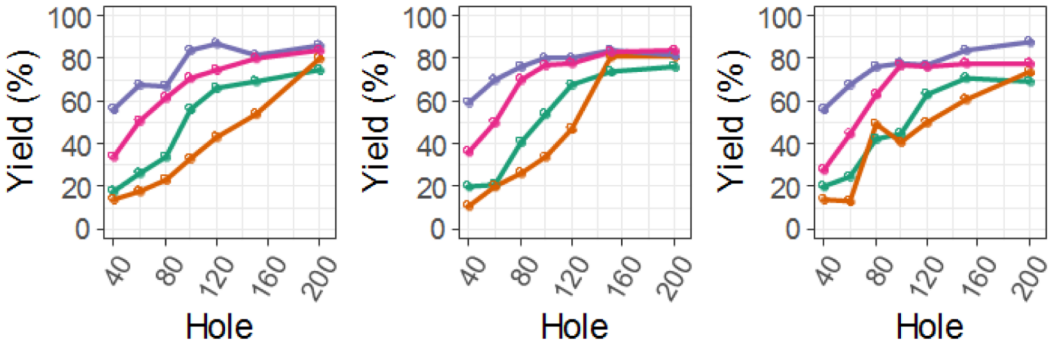
B-U growth: VLS growth of GaAs NW by MBE

- High yield of NW arrays on Si

- Key parameters:
  - Hole diameter
  - In and As fluxes
  - Temperature



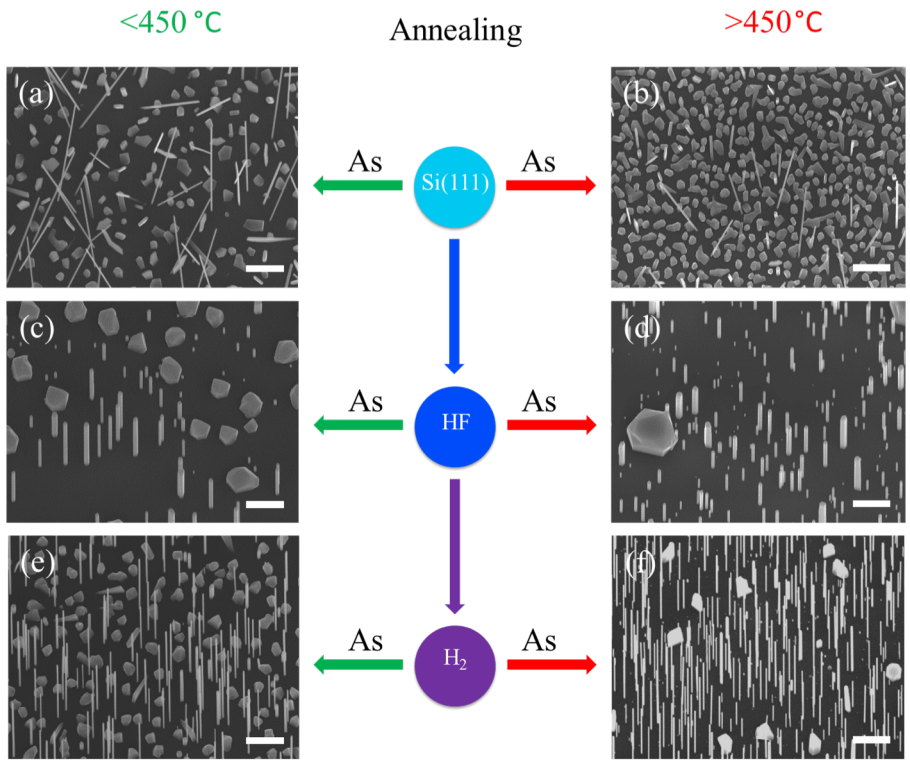
InAsSb

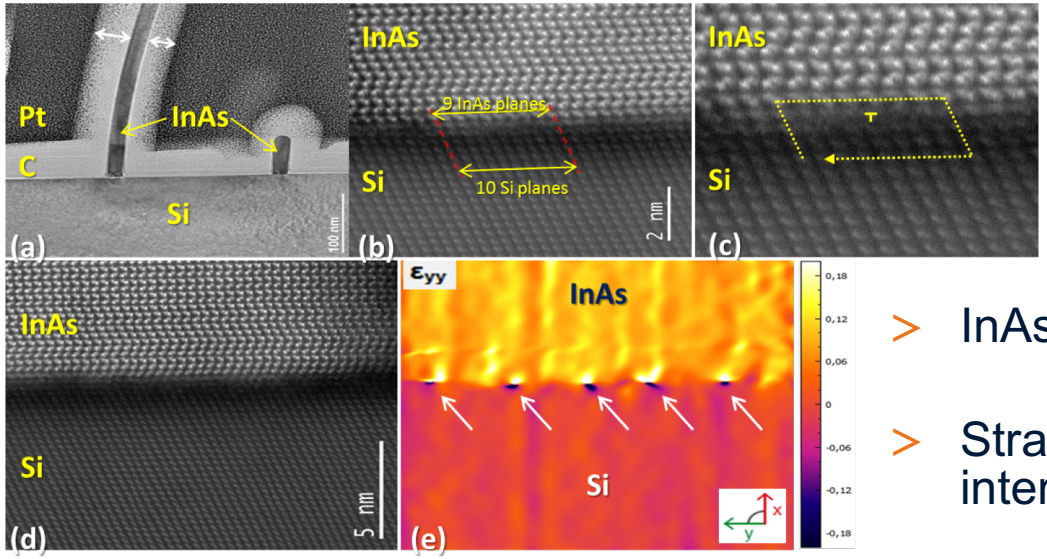


B-U: a CMOS compatible integration

> We developed a CMOS compatible process for the integration of high-mobility InAs nanowires on Silicon

In-situ annealing with As
+
HF 5%
+
H_2 plasma





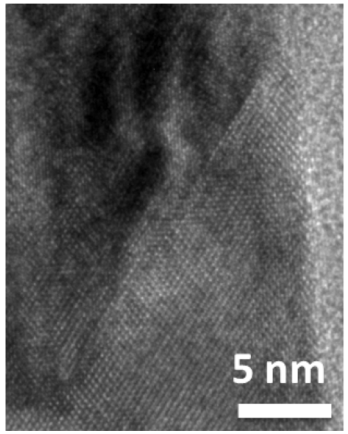
> InAs nanowires are epitaxially grown on Si(111)

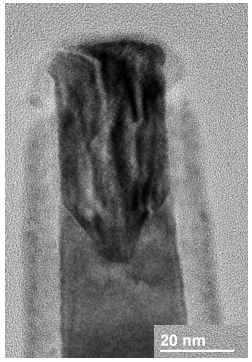
> Strain and dislocations are locked at the InAs-Si interface

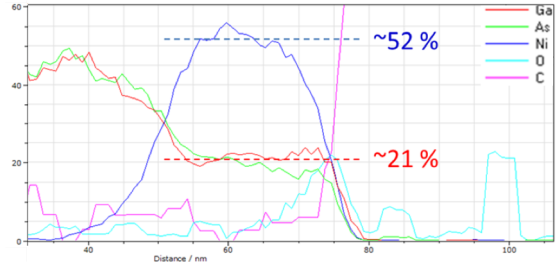
Integration issue on III-V: gate oxide and contacts

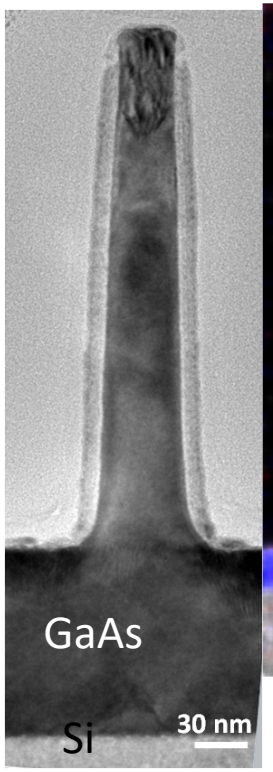
> 2 main roadblocks in III/V MOSFETs

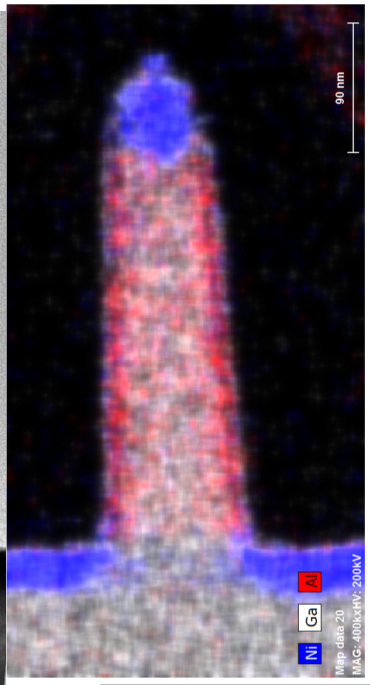
- Low resistive S/D contacts (CMOS comp)
- Gate oxide integration (low defects)

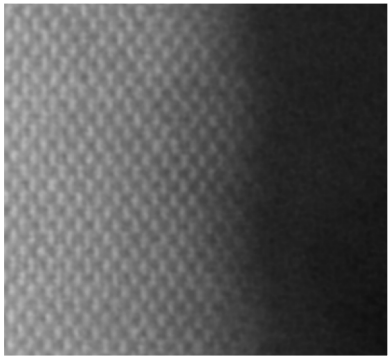


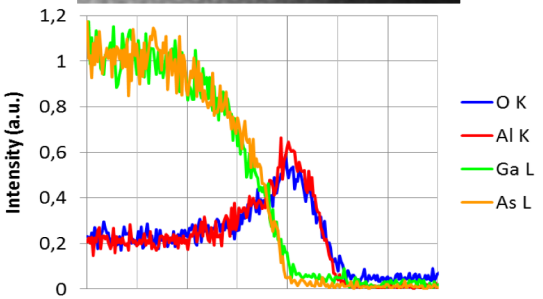












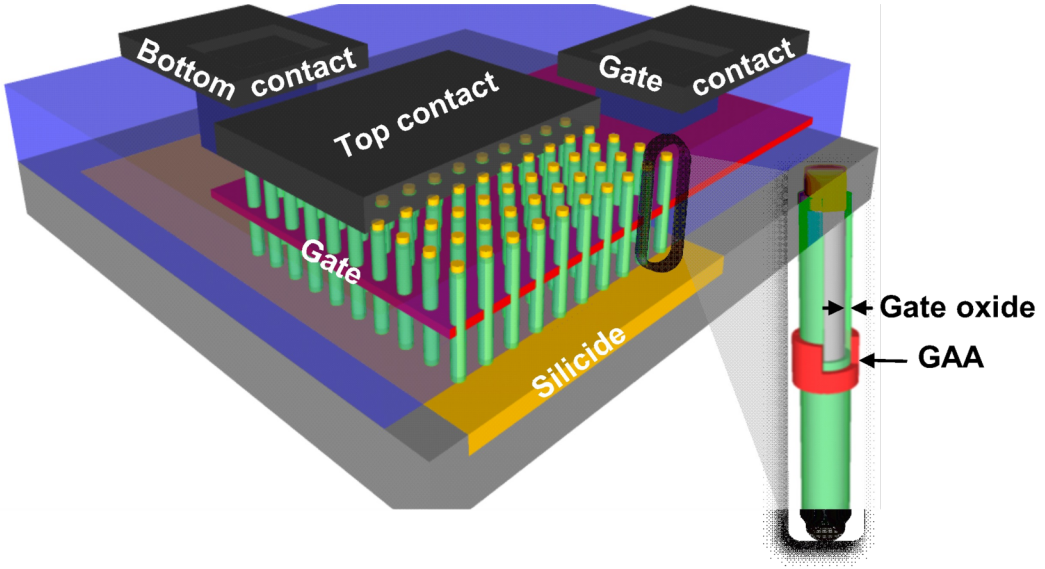
Low Resistive contacts on 3D NWs:
- Ni_2GaAs alloy (RTA anneal)
- CMOS-compatible technology
- Contact resistivity : 2.10^{-4} Ω .cm^{-2}

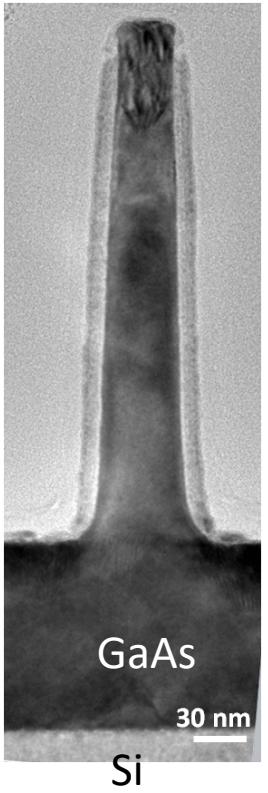
High-k gate oxide:
- Conformal Al_2O_3 layer by ALD
- Surface preparation : sulfur passivation + in-situ cleaning
- Interface defect density: 5.10^{12} $cm^{-2}.eV^{-1}$
- Oxide trapped charge : 2.10^{12} .cm^{-2}

Toward the full device demonstration

> Low power demo targeted:

- VDD ~ 0.5V
- Physical gate length < 15nm



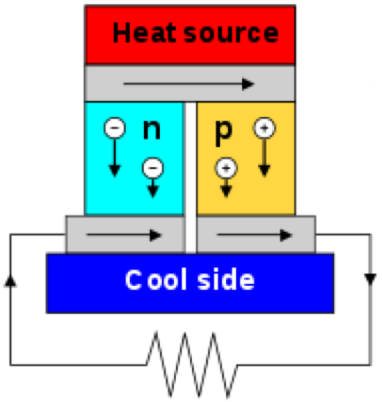


Other Opportunities: Thermoelectrics

> What is thermoelectricity ?

- A direct conversion of temperature gradients into electricity

(Seebeck effect)



> Why is it interesting ?

- Everywhere energy is used a part is "lost" in heat

(computers, cars, industry …)

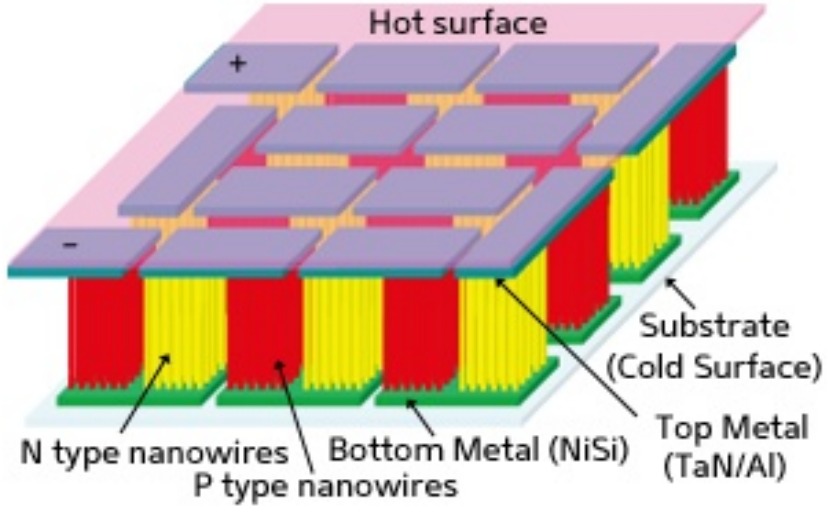
⇒ The idea is to "collect" these loses

> Nano-generators ?

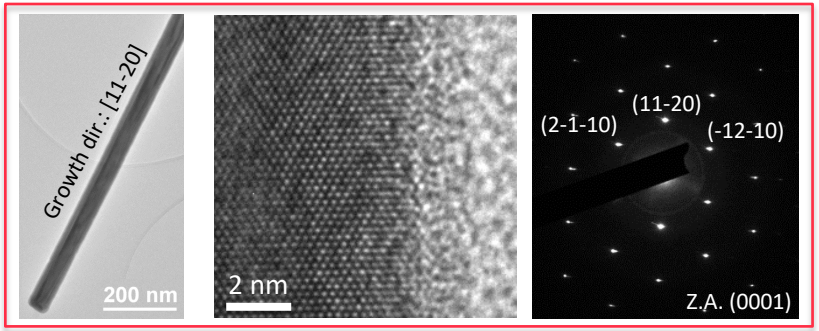
- Better performances than bulk (improved ZT) due to a lower thermal conductivity in NWs
- Interesting for "local" production

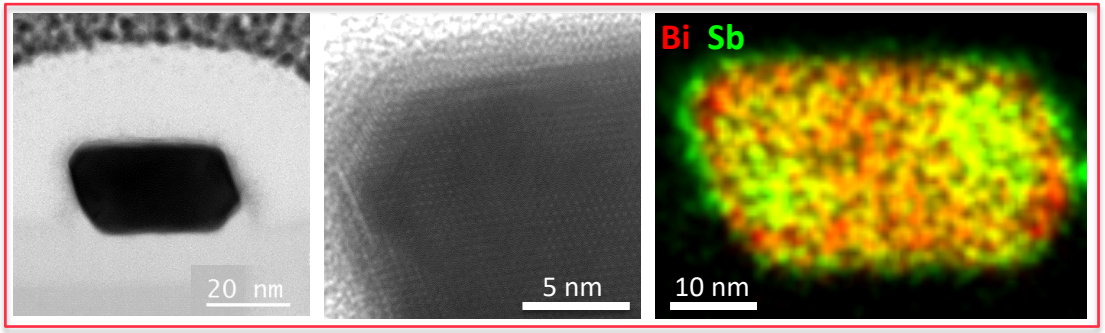
Other Opportunities: Thermoelectrics

> Using material engineering integrated on Si …



BiSb NWs





> … and developing new nanoscale Topological Insulators

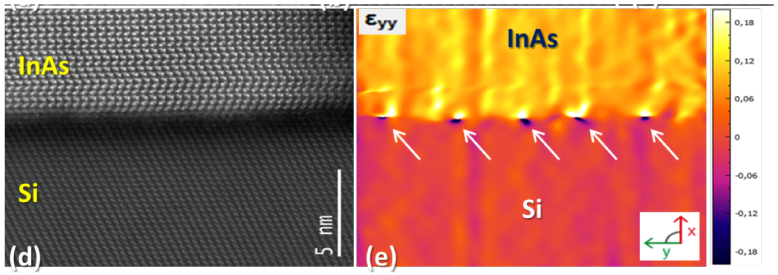
(near zero electrical resistance + high thermal resistance = high ZT)

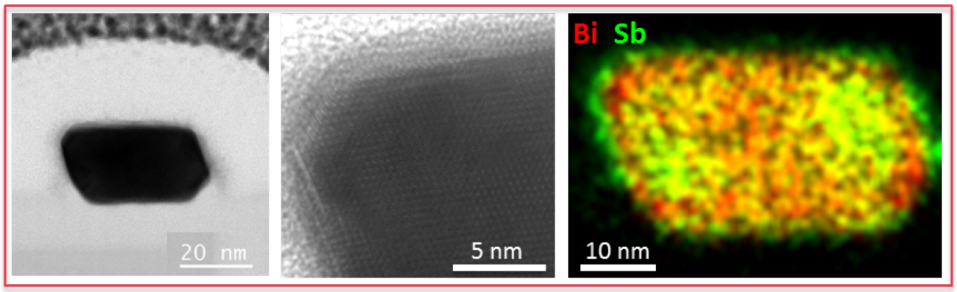
for improved thermoelectric devices

Conclusion

> III-V nanowires devices for energy:

- low power nanoelectronics : vertical III/V nanowires FETs: from NWs patterning to integration issues.
- Other opportunities: Thermoelectric …



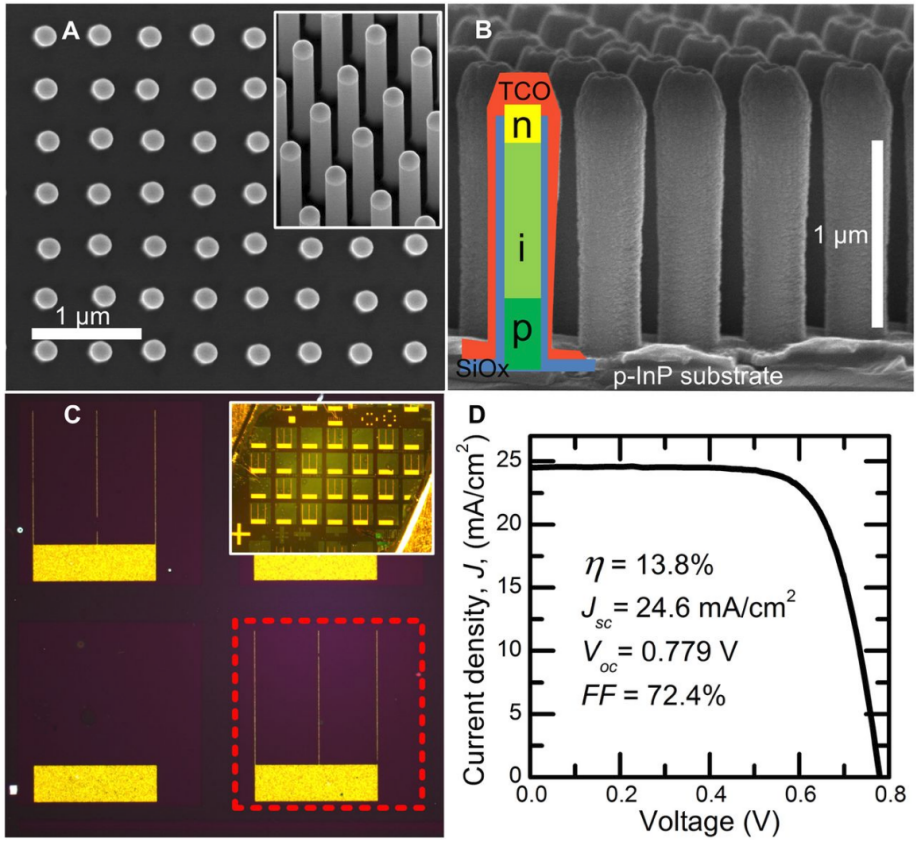


People involved in this thematic at LAAS:
Nicolas Mallet, Daya Dhungana, Aurélie Lecestre, Fuccio Cristiano, Pier Francesco Fazzini, Emmanuel Scheid, Julien Pezard, Sébastien Plissard, Guilhem Larrieu

Other Opportunities : Solar cells

InP Nanowire Array Solar Cells Achieving 13.8% Efficiency by Exceeding the Ray Optics Limit

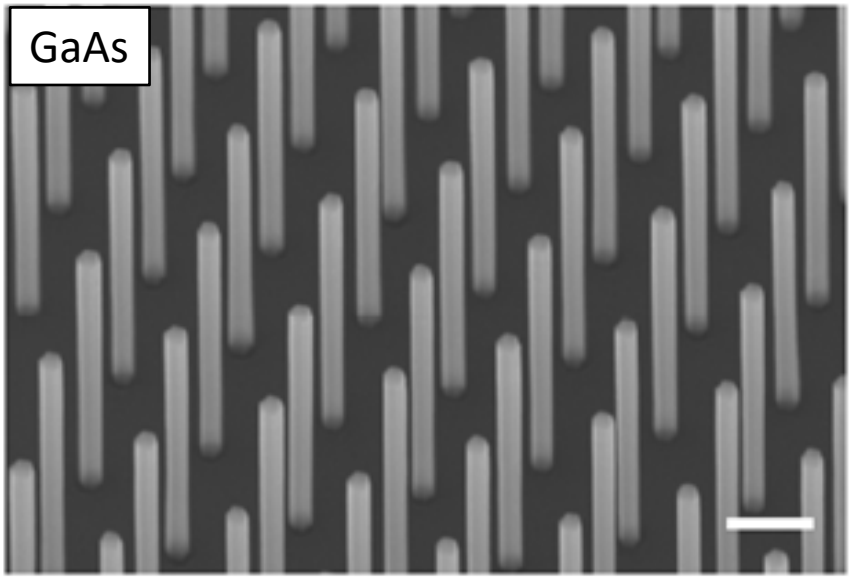
Jesper Wallentin,[1] Nicklas Anttu,[1] Damir Asoli,[2] Maria Huffman,[2] Ingvar Åberg,[2] Martin H. Magnusson,[2] Gerald Siefer,[3] Peter Fuss-Kailuweit,[3] Frank Dimroth,[3] Bernd Witzigmann,[4] H. Q. Xu,[1,5] Lars Samuelson,[1] Knut Deppert,[1] Magnus T. Borgström[1]*



Sciencexpress/ http://www.sciencemag.org/content/early/recent / 17 January 2013 / Page 1/ 10.1126/science.1230969

State of the art for NW solar cells

> Using III-V nanowires integrated on Si to build tandem solar cells



Using processes developed in LAAS for direct integration on silicon